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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1 53(b))

Attorney Docket No.	042390.P7511
First Inventor or Application Identifier	Ali Keshavarzi
Title	DECOUPLING CAPACITORS FOR THIN GATE OXIDES
Express Mail Label No.	EL034433717US

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents

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1. ☒ Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)
2. ☒ Specification [Total Pages 17]
(preferred arrangement set forth below)
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. ☒ Drawing(s) *(35 U.S.C. 113)* [Total Sheets 5]
4. Oath or Declaration [Total Pages 4]
   a. ☐ Newly executed (original copy)
   b. ☐ Copy from a prior application (37 C.F.R. § 1.63(d)) *(for continuation/divisional with Box 16 completed)*
      i. ☐ DELETION OF INVENTOR(S)
      Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR §§ 1.63(d)(2) and 1.33(b).

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ACCOMPANYING APPLICATION PARTS

7. ☐ Assignment Papers (cover sheet & document(s))
8. ☐ 37 C.F.R. § 3.73(b) Statement *(when there is an assignee)* ☐ Power of Attorney
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UNITED STATES PATENT APPLICATION

for

DECOUPLING CAPACITORS FOR THIN GATE OXIDES

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Docket No.: 42390.P7511

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"Express mail" label no. EL034433717US

DECOUPLING CAPACITORS FOR THIN GATE OXIDES

Background of the Invention

Technical Field of the Invention: The present invention relates to integrated circuits and, more particularly, to decoupling capacitors in integrated circuits.

Background Art: Decoupling capacitors ("decaps") are used in integrated circuit (IC) design for noise decoupling. Indeed, they are heavily used in virtually all IC's. One type of semiconductor capacitor is called a MOS-C or metal oxide semiconductor capacitor. The MOS-C has two terminals separated by a dielectric region (which includes at least an insulator, such as gate oxide). One of the terminals is the gate and the other is the body (and perhaps source and drain diffusions). Another type of semiconductor capacitor is using a field effect transistor (FET) such as an n-channel metal oxide semiconductor FET (NMOSFET) or a p-channel metal oxide semiconductor FET (NMOSFET). One of the terminals is the gate and the other terminal is the source, drain, and body. The terminals are separated by a dielectric (which includes at least an insulator, such as gate oxide). A difference between a MOS-C and a FET capacitor are that with a FET, the source and drains have a different polarity type than does the body. With a MOS-C, the source/ drain diffusions (if present) have the same polarity as the body. The behavior of capacitors in integrated circuits is described in R. Pierret et al., "Field Effect Devices," (Addison-Wesley, 2nd Ed. 1990), pp. 47-59; and in N. Weste et al., "Principles of CMOS VLSI Design," (Addison-Wesley, 2nd Ed. 1993), pp. 180-82.

Other decoupling capacitors such as a capacitor sandwiched in between two metal lines with a high dielectric constant insulator are also possible. However, the material challenge and integration in today's MOS technology will be very difficult.

The capacitance C of a capacitor is given by the equation $C = \varepsilon A/d$, were ε is the dielectric constant, A is the area, and d is the distance. In the design IC's, it is desirable to make the dimensions of the components small. Accordingly, over the years, the area A of the capacitors has become smaller, while the distance d between electrodes has also become smaller. Currently used capacitor structures generally work fairly well with oxides that do not leak. The current decoupling capacitors structures have voltages applied to keep the MOS-C in inversion

resulting in maximum per unit area capacitance value, with good high frequency response time, and low series resistance. As process technology scales, gate oxide thickness also scales in order to maintain transistors with good drive current capabilities and a good short channel behavior. As gate oxides continue to scale (e.g., below 30A), this capacitive configuration results in high leakage conduction through oxide (e.g., elevated tunneling leakage).

Summary

In some embodiments, the invention includes a die having a first conductor carrying a power supply voltage and a second conductor carrying a ground voltage. A semiconductor capacitor operating in depletion mode is coupled between the first and second conductors to provide decoupling capacitance between the first and second conductors, the semiconductor capacitor having a gate voltage.

Various configurations may be used including: n+ gate poly and n+ source/drain regions in an n-body; p+ gate poly and n+ source/drain regions in an n-body; p+ gate poly and p+ source/drain regions in an n-body; p+ gate poly and p+ source/drain regions in a p-body; n+ gate poly and p+ source/drain regions in a p-body; n+ gate poly and n+ source/drain regions in a p-body. The power supply voltage may have a larger absolute value than does a flatband voltage.

Additional embodiments are described and claimed.

Brief Description of the Drawings

The invention will be understood more fully from the detailed description given below and from the accompanying drawings of embodiments of the invention which, however, should not be taken to limit the invention to the specific embodiments described, but are for explanation and understanding only.

FIG. 1 is a schematic cross-sectional representation of a prior art capacitor.

FIG. 2 is a graphical representation of a capacitance v. gate-to-body voltage for capacitors with n-bodies with a zero work function.

FIG. 3 is a graphical representation of a capacitance v. gate-to-body voltage for capacitors with n-bodies with a non-zero work function.

FIG. 4 is a schematic cross-sectional representation of a capacitor according to some embodiments of the invention.

FIG. 5 is a schematic cross-sectional representation of a capacitor according to some embodiments of the invention.

FIG. 6 is a schematic cross-sectional representation of a capacitor according to some embodiments of the invention.

FIG. 7 is a graphical representation of a capacitance v. gate-to-body voltage for capacitors with p-bodies with a zero work function.

FIG. 8 is a graphical representation of a capacitance v. gate-to-body voltage for capacitors with p-bodies with a non-zero work function.

FIG. 9 is a schematic cross-sectional representation of a prior art capacitor.

FIG. 10 is a schematic cross-sectional representation of a capacitor according to some embodiments of the invention.

FIG. 11 is a schematic cross-sectional representation of a capacitor according to some embodiments of the invention.

FIG. 12 is a schematic cross-sectional representation of a capacitor according to some embodiments of the invention.

FIG. 13 is a block diagram representation of a die with a capacitor according to some embodiments of the invention.

FIG. 14 is a block diagram representation of a die with a capacitor and voltage circuitry according to some embodiments of the invention.

Detailed Description

The invention involves operating semiconductor capacitors (transistor or MOS-C) in a depletion mode to reduce leakage through the insulator (e.g., gate oxide). This is counter-intuitive because operating in the depletion mode reduces the capacitance per area. To make up for this reduction in capacitance, the area may be made bigger, which is undesirable. In the creation of the invention, the inventors noticed that by operating in the depletion mode, the

number of carriers is smaller, so there will be a smaller amount of tunneling in the gate oxide and hence less leakage.

In general, the idea is to move away from using a MOS-C capacitor derived from a MOS transistor structure operating in inversion mode. The alternative suggestion is to use a capacitor structure using the gate oxide as an insulator operating in depletion mode. Effective capacitance reduces by about 25% (approximated) while leakage reduces by approximately a factor of 100 for approximately a 1V power supply technology. Capacitance reduction is observable in the C-V curve as the capacitor is biased in a depletion mode (close to accumulation region). The leakage reduction is due to the fact that we have less carriers in depleted channel under the gate oxide to tunnel through the thin gate oxide. The Q-factor of such capacitor will be similar to a MOS transistor cap in inversion specially if we do not rely on minority carrier generation and recombination to provide the carriers need to respond to the AC signal superimposed on the decap. We can always compensate for the reduced capacitance by using slightly larger area capacitor if we have to lower the leakage through the decap by more than an order of magnitude.

<u>Decoupling capacitors with n-body.</u>

Referring to FIG. 1, a prior art PMOS transistor capacitor 10 includes a p-substrate, n-well, a p+ source S, a p+ drain D, p+ polysilicon gate electrode (poly) G, and an n+ body tap BT for a body B. According to the terminology of the present disclosure, transistor capacitor 10 is called a p+/p+ cap on n-body (n-well), where the first p+ signifies the poly type and the second p+ signifies the type of the S/D regions. Note that in the case of a capacitive structure is not particularly meaningful to call one diffusion region a source and the other a drain, but it is done for convenience in nomenclature. Note that source/drain diffusions are not necessary in every embodiment of the invention, however, they may reduce series resistance to help with the RC frequency response. A surface 12 is immediately beneath the gate oxide. A channel Ch is under the surface of the gate oxide. In the present disclosure, that area will be called a channel, even in the case of a MOC-C structure, which is not a transistor. Transistor capacitor 10 has voltage applied as follows: the body voltage Vb is at the power supply voltage Vcc (sometimes called Vdd), the source and drain voltages Vs and Vd are both Vcc, and the gate voltage V_G and the p-substrate are both at ground (called Vss or 0). The substrate can be grounded from beneath,

above, or elsewhere. In FIG. 1, Vg is tied to Vss. In some embodiments, however, G might not be tied to Vss and might be a non-zero and non-Vcc value.

FIG. 2 illustrates a capacitance vs. gate-to-body voltage V_{GB} curve for n-body (e.g., n-well) capacitive structures with a zero work function because the poly and body have the same type. Note that a drain and source voltage may be the same as the body voltage. The curve is intended to only show general relationships, not precise values or shapes. The actual curve could look somewhat different. Further, the shape of the curve may change at different frequencies. As can be seen, the capacitance is higher in accumulation and inversion and is lower in depletion. Vt is a threshold voltage. Generally, although the boundaries between accumulation, depletion, and inversion modes may be inexact, accumulation mode occurs when $0 < V_{GB}$, depletion mode occurs when $-Vt < V_{GB} < 0$, and inversion mode occurs when $V_{GB} < -Vt$.

FIG. 3 illustrates a capacitance vs. gate-to-body voltage V_{GB} curve for n-body capacitive structures with a non-zero work function (non-zero flat band voltage V_{FB}.) because the poly and body have a different type. The curve is intended to only show general relationships, not precise values or shapes. The actual curve could look somewhat different. Further, the shape of the curve may change at different frequencies. As can be seen, the capacitance is higher in accumulation and inversion and is lower in depletion. V_{FB} for a heavily doped poly is approximately 1.0 volts. Generally, although the boundaries between accumulation, depletion, and inversion modes may be inexact, accumulation mode occurs when $V_{FB} < V_{GB}$, depletion mode occurs when $-Vt < V_{GB} < V_{FB}$, and inversion mode occurs when $V_{GB} < -Vt$. Note that the relative distance between -Vt and 0 and between 0 and V_{FB} between 0 and Vt is not intended to be restrictive on actual values of V_{FB} or Vt, which may vary from embodiment to embodiment.

Consider the case of prior art transistor capacitor 10 of FIG. 1. The curve of FIG. 3 would apply because there is an n-body and the poly and body have different types, so there is a non-zero work function. The flatband voltage (V_{FB}) of this structure is approximately 1V. In the case of FIG. 1, V_{GB} = -Vcc, which is more negative than is -Vt. Therefore, transistor capacitor 10 is in the inversion mode (more specifically, the channel is in inversion because it includes holes which are an opposite type of the body). Accordingly, it has a very high (perhaps a maximum) capacitance per unit area, very good frequency response and low series resistance.

However, it also has leakage through gate oxide, especially for thin gate oxides is also high (perhaps a maximum). Vcc should be greater than Vt for this decap configuration. Note that the capacitance as a function of frequency and resistance in series with the cap (for displacement current) are representative of the Q-factor of the decap. Note that the flatband voltage (V_{FB}) is about 1V (not zero) for the PMOS cap in inversion because p+ poly gate and n-body.

FIG. 4 illustrates a MOS-C 40 according to some embodiments of the invention. Note that the term MOS (metal oxide semiconductor) is intended to be interpreted broadly where the metal is not restricted to any particular type of conductor (i.e., it does not have to be polysilicon), an insulator does not have to have an oxide, and the semiconductor portion is not restricted to a particular type of structure. MOS-C 40 is designated n+/n+ on n-body, according to the above described nomenclature (i.e., poly is n+, S/D is n+). Vg is Vcc and S/D/B are at 0 (Vss). The curve of FIG. 2 will apply because an n-well is used and the poly and body have the same type. V_{FB} of MOS-C 40 is 0V. V_{GB} = Vcc, so MOS-C 40 is in the accumulation mode (the channel is accumulated by electrons, which are the same type as the body). With the configuration of FIG. 4, it may be desirable to allow such a layout (drawing n-poly on n-well) in design tools. MOS-C 40 works with all Vcc values. It has high (good) capacitance per unit area at slightly lower leakage. It has good frequency response and low series resistance.

FIG. 5 illustrates MOS-C 50 according to some embodiments of the invention. MOS-C 40 is designated p+/n+ on n-body, according to the above described nomenclature. Vg is Vcc and S/D/B are at 0 (Vss). The curve of FIG. 3 will apply because an n-well is used and the poly and body have a different type. V_{FB} of MOS-C 50 is approximately 1V. V_{GB} = Vcc. If Vcc > V_{FB}, then MOS-C 50 is in the accumulation mode (channel accumulates) and if MOS-C < V_{FB}, then MOS-C 40 is in the depletion mode (channel depletes). When Vcc = V_{FB}, the mode is between accumulation and depletion mode. In some embodiments of the present invention, Vcc is less than V_{FB} so that MOS-C 50 will be in the depletion mode and leakage will be reduced. This configuration may require special layout. MOS-C 50 has lower capacitance per unit area but with much lower leakage because of the depletion mode (there are fewer carriers to leak). It has good frequency response, but may have high series resistance. Note that the structure resembles the buried channel MOS transistor structure.

FIG. 6 illustrates a PMOS transistor capacitor 60 MOS-C 60 according to some embodiments of the invention. Transistor capacitor 60 is designated p+/p+ on n-body, according to the above described nomenclature. Vg is Vcc and S/D/B are at 0 (Vss) (opposite of FIG. 1). The curve of FIG. 3 will apply because an n-well is used and the poly and body have a different type. V_{FB} of MOS-C 50 is approximately 1V. V_{GB} = Vcc. If Vcc > V_{FB}, then MOS-C 60 is in the accumulation mode (channel accumulates) and if MOS-C < V_{FB}, then MOS-C 60 is in the depletion mode (channel depletes). In some embodiments of the present invention, Vcc is less than V_{FB} so that MOS-C 60 will be in the depletion mode and leakage will be reduced. MOS-C 60 has lower capacitance per unit area but with much lower leakage because of the depletion mode (there are fewer carriers to leak). However, frequency response and series resistance may be an issue.

Decoupling capacitors with p-body.

The following describe examples of transistors and MOS-C capacitive structures with p-bodies (p-well or p-substrate). Note that although p-wells are shown the body could be just the p-substrate. Further, the substrate could be an n-type with a p-well.

FIG. 7 illustrates a capacitance vs. gate-to-body voltage V_{GB} curve for p-body capacitive structures with a zero work function because the poly and body have the same type. The curve is intended to only show general relationships, not precise values or shapes. The actual curve could look somewhat different. Further, the shape of the curve may change at different frequencies. As can be seen, the capacitance is higher in accumulation and inversion and is lower in depletion. Generally, although the boundaries between accumulation, depletion, and inversion modes may be inexact, accumulation mode occurs when $V_{GB} < 0$, depletion mode occurs when $0 < V_{GB} < Vt$, and inversion mode occurs when $V_{GB} > Vt$.

FIG. 8 illustrates a capacitance vs. gate-to-body voltage V_{GB} curve for p-body capacitive structures with a non-zero work function (non-zero flat band voltage V_{FB}.) because the poly and body have a different type. The curve is intended to only show general relationships, not precise values or shapes. The actual curve could look somewhat different. Further, the shape of the curve may change at different frequencies. As can be seen, the capacitance is higher in accumulation and inversion and is lower in depletion. V_{FB} for a heavily doped poly is

approximately 1.0 volts (although it is in the negative region of the curve). Generally, although the boundaries between accumulation, depletion, and inversion modes may be inexact, accumulation mode occurs when $V_{GB} < -V_{FB}$ (e.g., -1v), depletion mode occurs when $-V_{FB} < V_{GB} < Vt$, and inversion mode occurs when $Vt < V_{GB}$. Note that the relative distance between $-V_{FB}$ and 0 and between 0 and Vt is not intended to be restrictive on actual values of V_{FB} or Vt, which may vary from embodiment to embodiment.

FIG. 9 illustrates a prior art NMOS transistor capacitor 90 designated is designated n+/n+ on p-body, according to the above described nomenclature. In this case, it is a p-body is a p-substrate, but it could be a p-well on an n-substrate or a p-well in a p-substrate. Vg = Vcc and S/D/B are 0 (Vss). Since the poly and body have a different type, the curve of FIG. 8 is used. V_{GB} = Vcc. On curve 8, Vcc is greater than Vt, so transistor capacitor 90 is operating in inversion mode (the channel is in inversion). Decap 90 does not require a triple well process and uses no special layout requirements. It has very high (perhaps a maximum) capacitance per unit area, very good frequency response and low series resistance. The main issue is that leakage through gate oxide specially for thin gate oxides is also high (perhaps a maximum). Vcc should be greater than Vt for this decap configuration.

FIG. 10 illustrates a MOS-C capacitor 100 with a p+/p+ on p-body configuration, according to the above nomenclature. Although a p-well is illustrated it is not necessary. Vg = 0 (Vss) and S/D/B = Vcc. Because the poly and body are the same type, the curve of FIG. 7 applies. V_{GB} = -Vcc, so that capacitor 100 is in accumulation mode (channel would be accumulated). In some embodiments, capacitor 100 includes an n-body or other insulator between the p-well and p-substrate. The purpose is to prevent the Vcc voltage from influencing the voltage of the substrate or other bodies. This triple well process may need to additional layout (drawing P-poly on P-well) in the design tools. Decap 100 works with all Vcc values. It has high (good) capacitance per unit area at slightly lower leakage. It has good frequency response and low series resistance.

FIG. 11 illustrates a MOS-C capacitor 110 with a n+/p+ on p-body configuration, according to the above-described nomenclature. Although a p-well is illustrated it is not necessary. Vg = 0 (Vss) and S/D/B = Vcc. Because the poly and body are a different type, the

curve of FIG. 8 applies. V_{GB} = -Vcc. If Vcc > V_{FB} (-Vcc < -V_{FB}), then capacitor 110 would be in accumulation mode (channel would be accumulated). If Vcc < V_{FB} (-Vcc > -V_{FB}), then capacitor 110 would be in depletion mode (channel would be depleted). To help with leakage, in some embodiments, the depletion mode is used. In some embodiments, capacitor 110 includes an n-body or other insulator between the p-well and p-substrate. Capacitor 110 has lower capacitance per unit area at much lower leakage. It has good frequency response, but high series resistance.

FIG. 12 illustrates an NMOS transistor 120 with a n+/n+ on a p-body configuration according to the above-described nomenclature. Although a p-well is illustrated it is not necessary. Vg = 0 (Vss) and S/D/B = Vcc. Because the poly and body are a different type, the curve of FIG. 8 applies. V_{GB} = -Vcc. If Vcc > V_{FB} (-Vcc < -V_{FB}), then capacitor 120 would be in accumulation mode (channel would be accumulated). If Vcc < V_{FB} (-Vcc > -V_{FB}), then capacitor 120 would be in depletion mode (channel would be depleted). To help with leakage, in some embodiments, the depletion mode is used. In some embodiments, capacitor 120 includes an n-body or other insulator between the p-well and p-substrate. Leakage is good (lower) in this configuration. However, frequency response and series resistance may be an issue. This configuration may require a triple well process.

An Appendix before the claims provides a comparison summary table for the above illustrated capacitors as wells as other capacitors within the scope of some embodiments of the invention.

Other Information and Embodiments

FIG. 13 illustrates a die 130 in which capacitors (e.g., capacitor 134) including one or more of the configurations described herein may be included. Die 130 may be any of a various types of electrical devices including a microprocessor, DSP (digital signal processor), embedded controller, ASIC (application specific integrated circuit), and communication chip.

As described above, in some embodiments, it is desirable to have a capacitor be in depletion mode. In many situations, it would also be desirable to have the capacitor be close to accumulation or inversion mode. Note that in FIGS. 2, 3, 7, and 8, in depletion mode the curve increases toward accumulation or inversion mode. It would be possible to tweak the capacitance

by adjusting the gate voltage, body voltage, source/drain voltage, threshold voltage, and/or doping levels. Referring to FIG. 14, a die 140 includes capacitor 134 (which is representative of one or more of the various capacitors described therein). Die 140 includes voltage circuitry 142, which can provide the voltage(s) for one or more of the body, gate, and source/drain to provide a desired capacitance level. Changing the body voltage may make a capacitor have a forward or reverse body bias. Note that Vt changes as the body bias changes. There may also be a feedback mechanism to obtain a desired capacitance level.

Merely as an example, in some embodiments, it is believed that effective capacitance may be reduced by approximately 25%, while leakage reduces by approximately a factor of 100 for approximately a 1V power supply technology. Capacitance reduction is observable in the C-V curve as the capacitor is biased in a depletion mode (close to accumulation region). The leakage reduction is due to there being fewer carriers in depleted channel under the gate oxide to tunnel through the thin gate oxide. The Q-factor of such capacitor will be similar to a MOS transistor cap in inversion specially if we do not rely on minority carrier generation and recombination to provide the carriers need to respond to the AC signal superimposed on the decap. We can compensate for the reduced capacitance by using slightly larger area capacitor if we have to lower the leakage through the decap by more than an order of magnitude. The invention accordingly supports additional supply voltage scaling and development of process technologies for low voltage, high performance and low power CMOS circuits. In the future, we can continue to utilize decaps for noise decoupling in our IC's with our proposed configuration even as we scale the gate oxide thickness required for the faster scaled transistors. Our proposed solution is compatible with current processing technology.

The invention may be used in connection with SOI (silicon on insulator) configurations.

Also, as is well known, power supply and ground voltages are not necessarily constant, but rather have fluctuations because of noise, load, or other reasons.

FETs other than MOSFETs could be used. Although the illustrated embodiments include enhancement mode transistors, depletion mode transistors could be used with modifications to the circuit which would be apparent to those skilled in the art having the benefit of this disclosure.

Reference in the specification to "an embodiment," "one embodiment," “some embodiments,” or "other embodiments" means that a particular feature, structure, or characteristic described in connection with the embodiments is included in at least some embodiments, but not necessarily all embodiments, of the invention. The various appearances "an embodiment," "one embodiment," or “some embodiments” are not necessarily all referring to the same embodiments.

If the specification states a component, feature, structure, or characteristic “may”, “might”, or “could” be included, that particular component, feature, structure, or characteristic is not required to be included. If the specification or claim refers to "a" or "an" element, that does not mean there is only one of the element. If the specification or claims refer to "an additional" element, that does not preclude there being more than one of the additional element.

Those skilled in the art having the benefit of this disclosure will appreciate that many other variations from the foregoing description and drawings may be made within the scope of the present invention. Accordingly, it is the following claims including any amendments thereto that define the scope of the invention.

Appendix: Comparison Summary Table listing some possibilities. This is not intended to be comprehensive. Other possibilities exist. Some of the information is merely a best guess.

Type	Vcc	Mode	Cap	Leakage	Hi freq	Rs	Comment
DeCap on n-well							
p+/p+ (prior art) (FIG. 1)	>Vt	inv	max	max	good	low	
n+/n+ (FIG. 4)	All	acc	~ max	slightly less	good	low	No LO
p+/p+ (FIG. 6)	<1V	dep	lower	lower	OK	high	No LO
p+/p+	>1V	acc	~ max	slightly less	OK	high	No LO
p+/n+ (FIG. 5)	<1V	dep	lower	lower	OK	high	LO
p+/n+	>1V	acc	~ max	slightly less	good	low	LO
n+/p+	>1V+Vt	inv	max	max	good	low	LO, Vcc ?
n+/p+	<1V+Vt	dep	lower	lower	OK	high	LO, Vcc ?
DeCap on p-well							
n+/n+ (prior art) (FIG. 9)	>Vt	inv	max	max	good	low	
p+/p+ (FIG. 10)	All	acc	~ max	slightly less	good	low	No LO
n+/n+ (FIG. 12)	<1V	dep	lower	lower	OK	high	No LO, TW
n+/n+	>1V	acc	~ max	slightly less	OK	high	No LO, TW
n+/p+ (FIG. 11)	<1V	dep	lower	lower	OK	high	LO, TW
n+/p+	>1V	acc	~ max	slightly less	good	low	LO, TW
p+/n+	>1V+Vt	inv	max	max	good	low	LO, Vcc ?
p+/n+	<1V+Vt	dep	lower	lower	OK	high	LO, Vcc ?

Key:
p+/p+ on N-Well means a capacitor with p+ poly and p+ S/D regions on N-Well
No LO = No Layout or tool change required over conventional design
LO = May require layout change as compared to that of convention design
V_{FB} = ~ 1V used for Vcc column
TW = May use triple well to insulate body of capacitor

CLAIMS

What is claimed is:

1. A die, comprising:

a first conductor carrying a power supply voltage;

a second conductor carrying a ground voltage; and

at least one semiconductor capacitor operating in depletion mode coupled between the first and second conductors to provide decoupling capacitance between the first and second conductors, the at least one semiconductor capacitor having a gate voltage.

2. The die of claim 1, wherein the at least one semiconductor capacitor has a n+ gate poly and n+ source/drain regions in an n-body.

3. The die of claim 1, wherein the at least one semiconductor capacitor has a p+ gate poly and n+ source/drain regions in an n-body.

4. The die of claim 1, wherein the at least one semiconductor capacitor has a p+ gate poly and p+ source/drain regions in an n-body.

5. The die of claim 1, wherein the at least one semiconductor capacitor has a p+ gate poly and p+ source/drain regions in a p-body.

6. The die of claim 1, wherein the at least one semiconductor capacitor has a n+ gate poly and p+ source/drain regions in a p-body.

7. The die of claim 1, wherein the at least one semiconductor capacitor has a n+ gate poly and n+ source/drain regions in a p-body.

8. The die of claim 1, wherein the power supply voltage has a smaller absolute value than does a flatband voltage.

9. The die of claim 1, further comprising voltage circuitry to provide a body voltage to the at least one semiconductor capacitor and wherein the gate voltage is provided by the first conductor.

10. The die of claim 1, further comprising voltage circuitry to provide a body voltage to the at least one semiconductor capacitor and wherein the gate voltage is provided by the second conductor.

11. The die of claim 1, further comprising voltage circuitry to provide the gate voltage and wherein a body voltage of the at least one semiconductor capacitor is provided by the first conductor.

12. The die of claim 1, further comprising voltage circuitry to provide the gate voltage and wherein a body voltage of the at least one semiconductor capacitor is provided by the second conductor.

13. The die of claim 1, further comprising additional capacitors between the first and second conductors at least some of which are not in the depletion mode.

14. A die, comprising:

a first conductor carrying a power supply voltage (Vcc);

a second conductor carrying a ground voltage (Vss); and

capacitors having:

(a) a conductive gate;

(b) an insulator dielectric;

(c) a semiconductor body,

wherein, the capacitor is in a depletion mode.

15. The die of claim 14, wherein the capacitors have a n+ gate poly and n+ source/drain regions in an n-body.

16. The die of claim 14, wherein the capacitors has a p+ gate poly and n+ source/drain regions in an n-body.

17. The die of claim 14, wherein the capacitors has a p+ gate poly and p+ source/drain regions in an n-body.

18. The die of claim 14, wherein the capacitors has a p+ gate poly and p+ source/drain regions in a p-body.

19. The die of claim 14, wherein the capacitors has a n+ gate poly and p+ source/drain regions in a p-body.

20. The die of claim 14, wherein the capacitors has a n+ gate poly and n+ source/drain regions in a p-body.

21. The die of claim 14, wherein the power supply voltage has a smaller absolute value than does a flatband voltage.

22. A die, comprising:

a first conductor carrying a power supply voltage;

a second conductor carrying a ground voltage; and

at least one semiconductor capacitor coupled between the first and second conductors to provide decoupling capacitance between the first and second conductors, the semiconductor capacitor having a gate voltage, the semiconductor capacitor having a flatband voltage and wherein the power supply voltage has a smaller absolute value than does the flatband voltage.

23. The die of claim 22, wherein the at least one semiconductor capacitor has a n+ gate poly and n+ source/drain regions in an n-body.

24. The die of claim 22, wherein the at least one semiconductor capacitor has a p+ gate poly and n+ source/drain regions in an n-body.

25. The die of claim 22, wherein the at least one semiconductor capacitor has a p+ gate poly and p+ source/drain regions in an n-body.

26. The die of claim 22, wherein the at least one semiconductor capacitor has a p+ gate poly and p+ source/drain regions in a p-body.

27. The die of claim 22, wherein the at least one semiconductor capacitor has a n+ gate poly and p+ source/drain regions in a p-body.

28. The die of claim 22, wherein the at least one semiconductor capacitor has a n+ gate poly and n+ source/drain regions in a p-body.

Abstract of the Disclosure

In some embodiments, the invention involves a die having a first conductor carrying a power supply voltage and a second conductor carrying a ground voltage. A semiconductor capacitor operating in depletion mode is coupled between the first and second conductors to provide decoupling capacitance between the first and second conductors, the semiconductor capacitor having a gate voltage. Various configurations may be used including: n+ gate poly and n+ source/drain regions in an n-body; p+ gate poly and n+ source/drain regions in an n-body; p+ gate poly and p+ source/drain regions in an n-body; p+ gate poly and p+ source/drain regions in a p-body; n+ gate poly and p+ source/drain regions in a p-body; n+ gate poly and n+ source/drain regions in a p-body. The power supply voltage may have a larger absolute value than does a flatband voltage.

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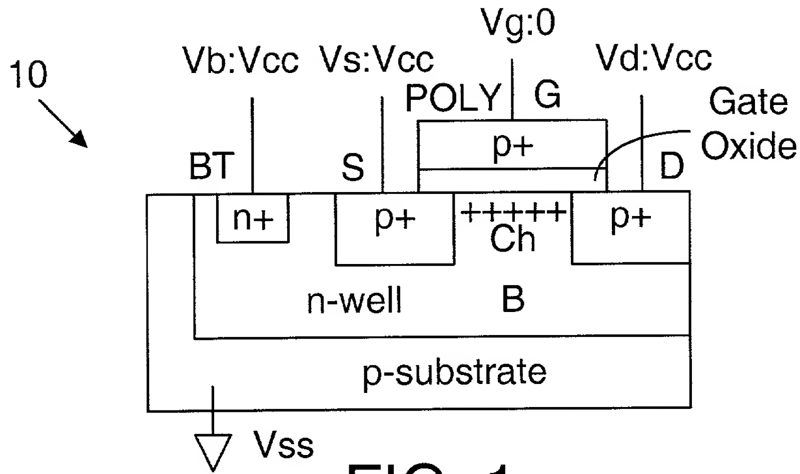


FIG. 1
(Prior Art)

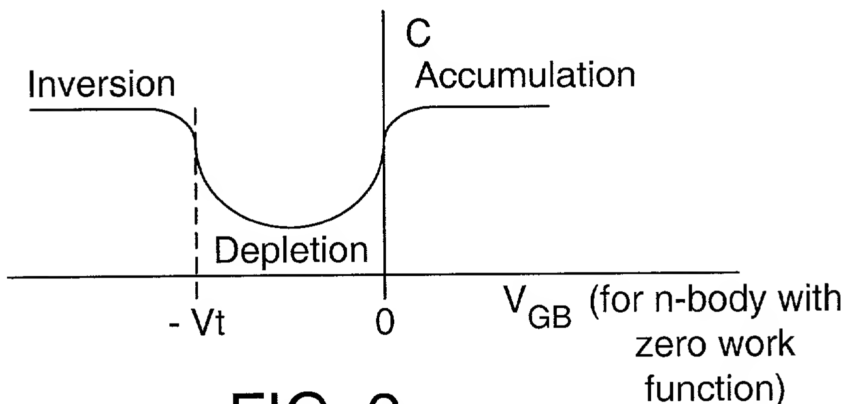


FIG. 2

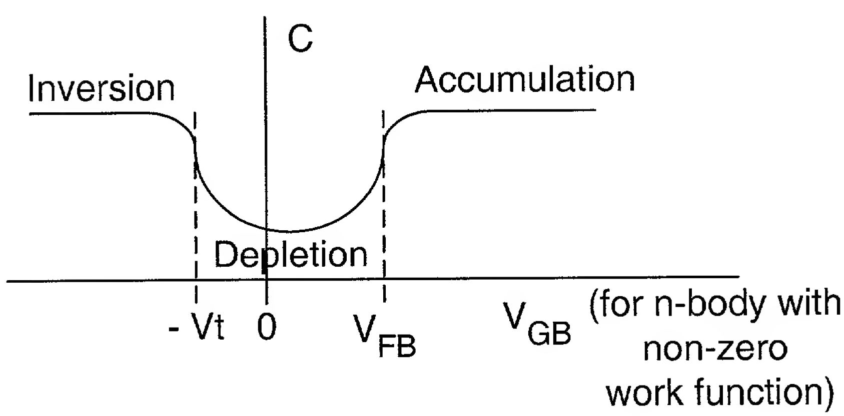


FIG. 3

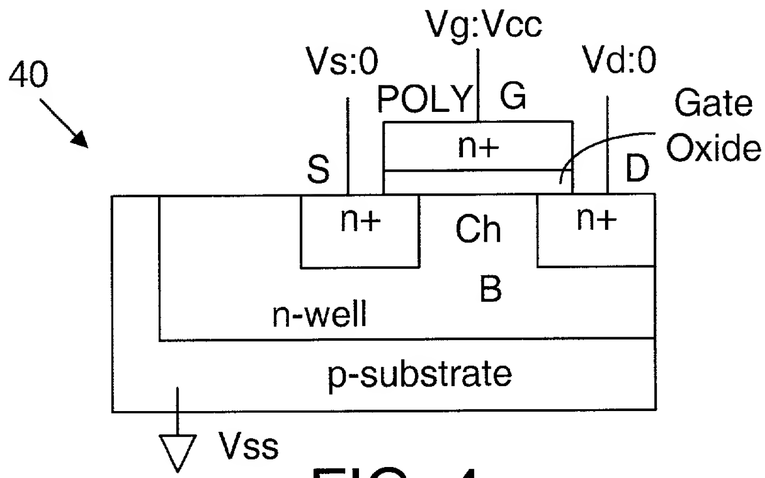


FIG. 4

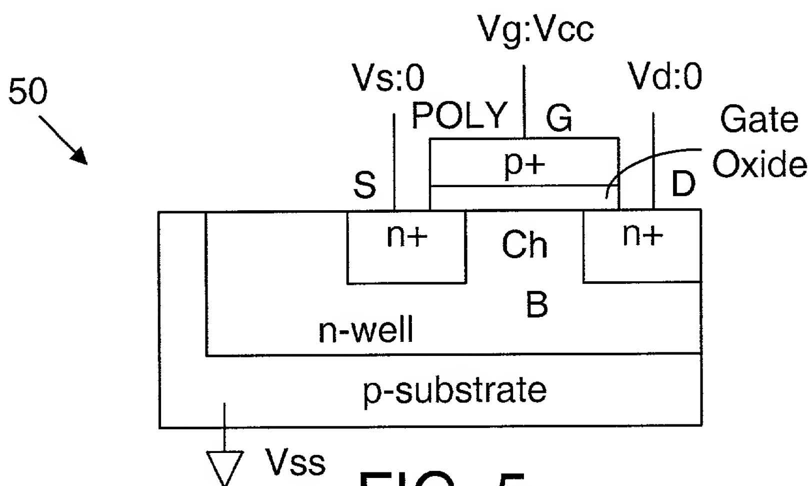


FIG. 5

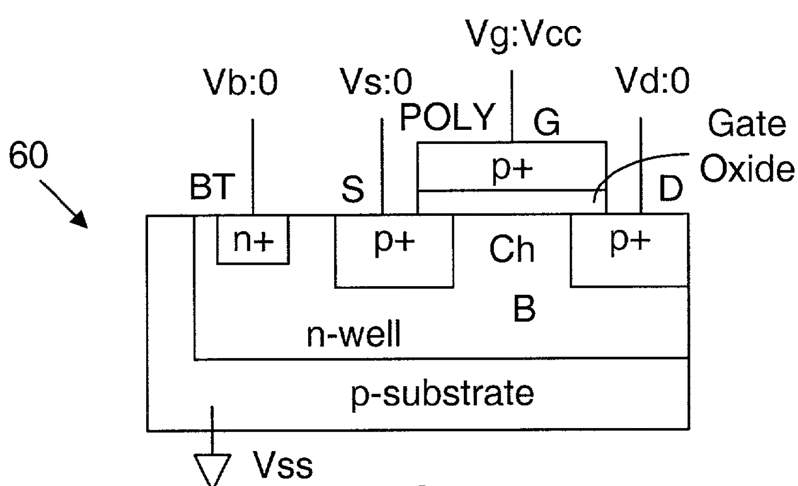


FIG. 6

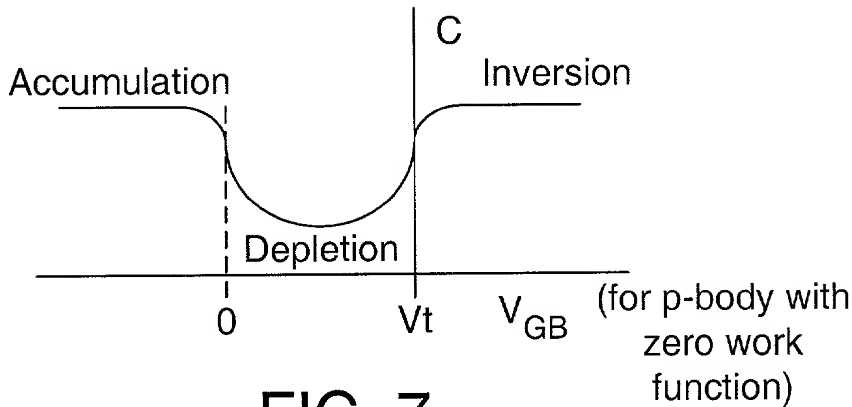


FIG. 7

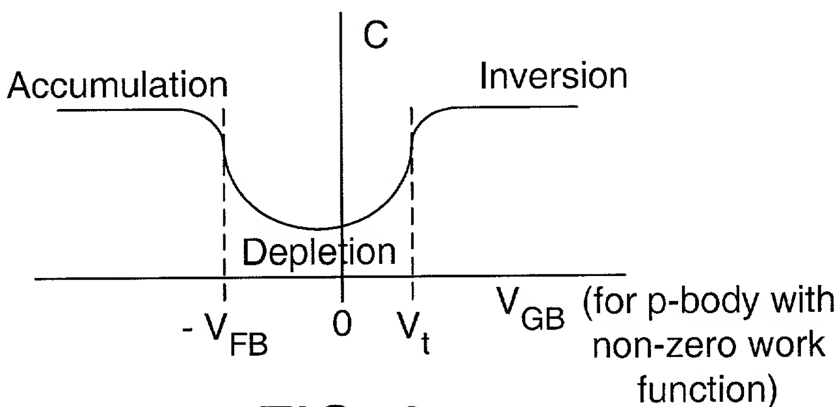


FIG. 8

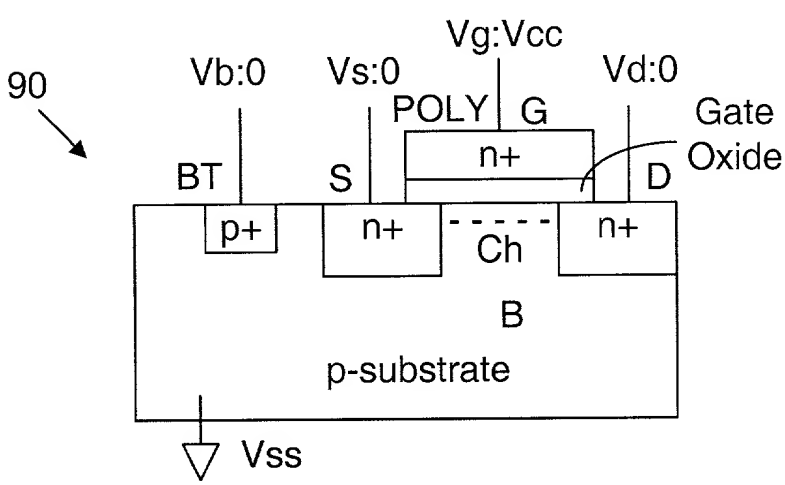
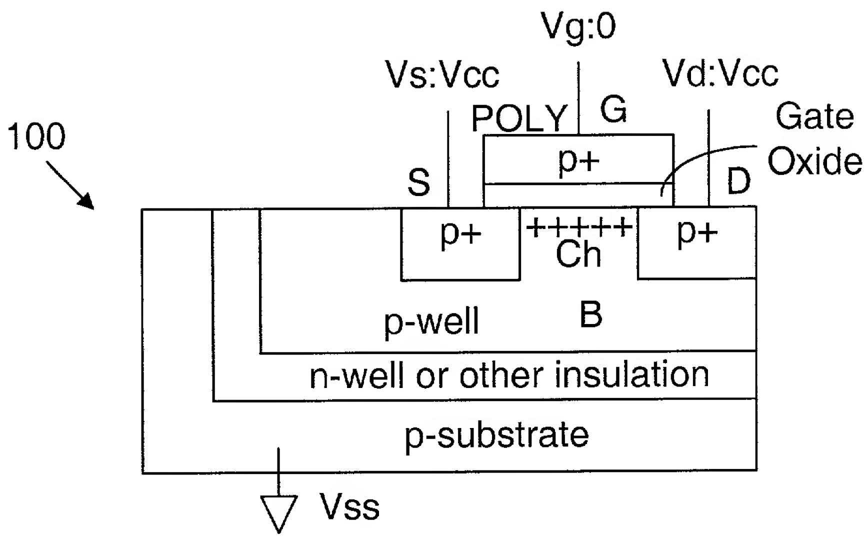
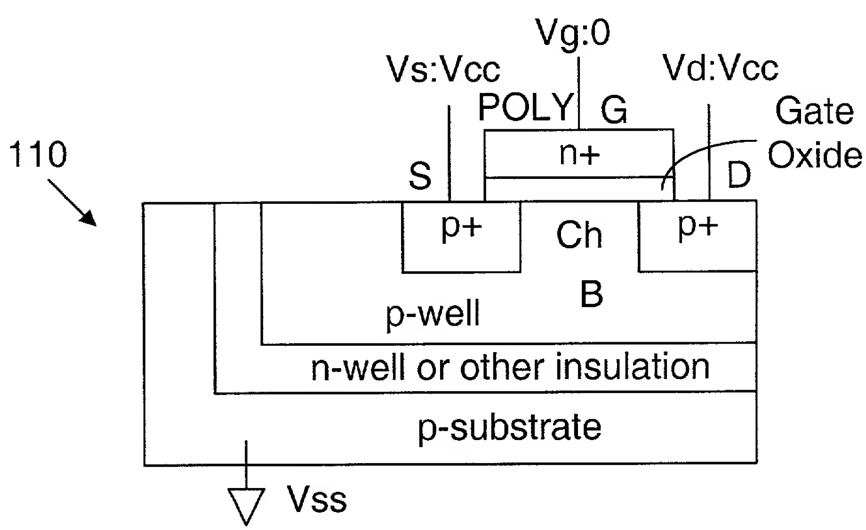


FIG. 9
(Prior Art)



Vg:0
Vs:Vcc
Vd:Vcc
POLY
G
Gate
Oxide
100
p+
S
D
p+
++++++
Ch
p+
p-well
B
n-well or other insulation
p-substrate
Vss

FIG. 10



Vg:0
Vs:Vcc
Vd:Vcc
POLY
G
Gate
Oxide
110
n+
S
D
p+
Ch
p+
p-well
B
n-well or other insulation
p-substrate
Vss

FIG. 11

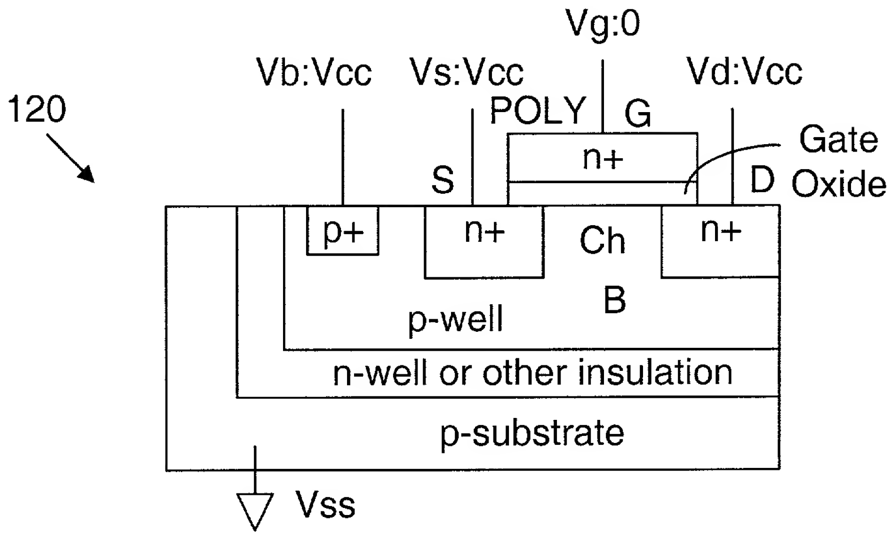


FIG. 12

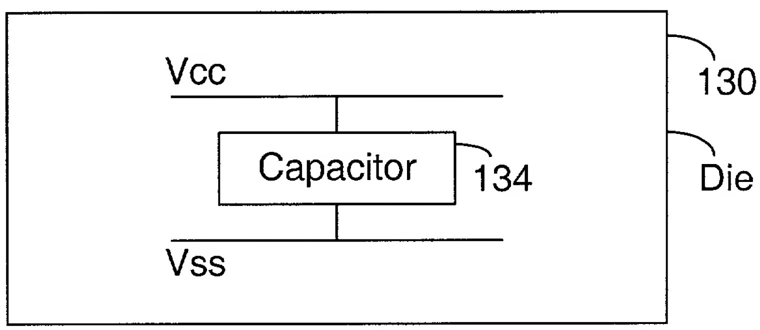


FIG. 13

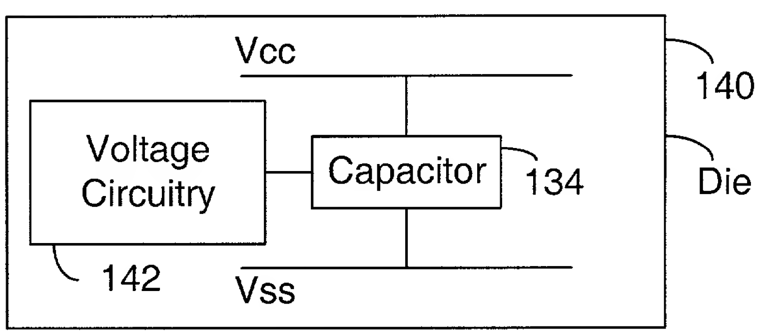


FIG. 14

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION
(FOR INTEL CORPORATION PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

DECOUPLING CAPACITORS FOR THIN GATE OXIDES

the specification of which

[X] is attached hereto.
[ ] was filed on ______________ as
United States Application Number ______________
or PCT International Application Number ______________
and was amended on ______________ .
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):

APPLICATION NUMBER	COUNTRY (OR INDICATE IF PCT)	DATE OF FILING (day, **month**, year)	PRIORITY CLAIMED UNDER 37 USC 119
			☐ No ☐ Yes
			☐ No ☐ Yes
			☐ No ☐ Yes

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

APPLICATION NUMBER	FILING DATE

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION NUMBER	FILING DATE	STATUS (ISSUED, PENDING, ABANDONED)

I hereby appoint BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, a firm including: William E. Alford, Reg. No. 37,764; Farzad E. Amini, Reg. No. P42,261; Aloysius T. C. AuYeung, Reg. No. 35,432; William Thomas Babbitt, Reg. No. 39,591; Carol F. Barry, Reg. No. 41,600; Jordan Michael Becker, Reg. No. 39,602; Bradley J. Bereznak, Reg. No. 33,474; Michael A. Bernadicou, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831, Gregory D. Caldwell, Reg. No. 39,926; Ronald C. Card, Reg. No. 44,587; Thomas M. Coester, Reg. No. 39,637; Donna Jo Coningsby, Reg. No. 41,684; Stephen M. De Klerk, under 37 C.F.R. § 10.9(b); Michael Anthony DeSanctis, Reg. No. 39,957; Daniel M. De Vos, Reg. No. 37,813; Robert Andrew Diehl, Reg. No. 40,992; Matthew C. Fagan, Reg. No. 37,542; Tarek N. Fahmi, Reg. No. 41,402; James Y. Go, Reg. No. 40,621; James A. Henry, Reg. No. 41,064; Willmore F. Holbrow III, Reg. No. P41,845; Sheryl Sue Holloway, Reg. No. 37,850; George W Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139; Dag H. Johansen, Reg. No. 36,172; William W. Kidd, Reg. No. 31,772; Erica W. Kuo, Reg. No. 42,775; Michael J. Mallie, Reg. No. 36,591; Andre L. Marais, under 37 C.F.R. § 10.9(b); Paul A. Mendonsa, Reg. No. 42,879; Darren J. Milliken, Reg. 42,004; Lisa A. Norris, Reg. No. P44,976; Chun M. Ng, Reg. No. 36,878; Thien T. Nguyen, Reg. No. 43,835; Thinh V. Nguyen, Reg. No. 42,034; Dennis A. Nicholls, Reg. No. 42,036; Kimberley G. Nobles, Reg. No. 38,255; Daniel E. Ovanezian, Reg. No. 41,236; Babak Redjaian, Reg. No. 42,096; William F. Ryann, Reg. 44,313; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Jeffrey Sam Smith, Reg. No. 39,377; Maria McCormack Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 25,128; Judith A. Szepesi, Reg. No. 39,393; Vincent P. Tassinari, Reg. No. 42,179; Edwin H. Taylor, Reg. No. 25,129; John F. Travis, Reg. No. 43,203; George G. C. Tseng, Reg. No. 41,355; Joseph A. Twarowski, Reg. No. 42,191; Lester J. Vincent, Reg. No. 31,460; Glenn E. Von Tersch, Reg. No. 41,364; John Patrick Ward, Reg. No. 40,216; Charles T. J. Weigell, Reg. No. 43,398; Kirk D. Williams, Reg. No. 42,229; James M. Wu, Reg. No. P45,241; Steven D. Yates, Reg. No. 42,242; Ben J. Yorks, Reg. No. 33,609; and Norman Zafman, Reg. No. 26,250; my patent attorneys, and Andrew C. Chen, Reg. No. 43,544; Justin M. Dillon, Reg. No. 42,486; Paramita Ghosh, Reg. No. 42,806; and Sang Hui Kim, Reg. No. 40,450; my patent agents, of BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (310) 207-3800, and Alan K. Aldous, Reg. No. 31,905; Robert D. Anderson, Reg. No. 33,826; Joseph R. Bond, Reg. No. 36,458; Richard C. Calderwood, Reg. No. 35,468; Jeffrey S. Draeger, Reg. No. 41,000; Cynthia Thomas Faatz, Reg No. 39,973; Sean Fitzgerald, Reg. No. 32,027; Seth Z. Kalson, Reg. No. 40,670; David J. Kaplan, Reg. No. 41,105; Charles A. Mirho, Reg. No. 41,199; Leo V. Novakoski, Reg. No. 37,198; Naomi Obinata, Reg. No. 39,320; Thomas C. Reynolds, Reg. No. 32,488; Kenneth M. Seddon, Reg. No. 43,105; Mark Seeley, Reg. No. 32,299; Steven P. Skabrat, Reg. No. 36,279; Howard A. Skaist, Reg. No. 36,008; Steven C. Stewart, Reg. No. 33,555; Raymond J. Werner, Reg. No. 34,752; Robert G. Winkle, Reg. No. 37,474; and Charles K. Young, Reg. No. 39,435; my patent attorneys, and Thomas Raleigh Lane, Reg. No. 42,781; Calvin E. Wells; Reg. No. P43,256, Peter Lam, Reg. No. P44,855; and Gene I. Su, Reg. No. 45,140; my patent agents, of INTEL CORPORATION; and James R. Thein, Reg. No. 31,710, my patent attorney; with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to Aloysius T.C. AuYeung, Reg. No. 35,432, BLAKELY, SOKOLOFF, TAYLOR &
(Name of Attorney or Agent)
ZAFMAN LLP, 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025 and direct telephone calls to Aloysius T.C. AuYeung, Reg. No. 35,432, (503) 684-6200.
(Name of Attorney or Agent)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Inventor's Signature ______________________ Date ____________

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Citizenship India
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Hillsboro, Oregon 97124 USA

Title 37, Code of Federal Regulations, Section 1.56
Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclosure information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclosure all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) Prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made or record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.